**Joseph Peters, WORK LOG**

**MILESTONE 1 WORK:**

Tuesday, January 14, 2020

Met with team [4 hr]

We decided on the architecture and planned out most of the components there-in. For example we decided on what registers were used for what, what instruction types to use, and how to implement the necessary instructions at the machine code and hardware levels.

My tasks for milestone 2 were to be decided at the next group meeting.

**MILESTONE 2 WORK:**

Tuesday, January 21, 2020

Met with team [2 hr]

We worked on implementing the RTL and started planning for the data path elements.

Wednesday, January 22, 2020

Worked on procedure call example and spec [1 hr]

My tasks for milestone 3 were to brainstorm for data path specifications and start writing part tests for datapath components.

**MILESTONE 3 WORK:**

Tuesday, January 28, 2020

Met with team [3 hr]

We worked on implementing the datapath for our processor. We also talked about which parts would need to be made and which people would make each part.

Wednesday, January 29, 2020

Worked on the alu for the lab due Friday. Also started working on the main alu [4 hr]

My tasks for milestone 4 were to finish the alu lab and create the alu for our processor along with the test cases.

**MILESTONE 4 WORK:**

Friday, February 3, 2020

Finished the alu lab and planned the 16b alu [3 hrs]

Tuesday, February 7, 2020

Worked on 16b alu [2 hrs]

Wednesday, February 8, 2020

Finished 16b alu with changes for our implementation [2 hrs]

My tasks for milestone 5 were to finish the test cases for the alu and to assist in piecing the datapath together.

**MILESTONE 5 WORK:**

Friday, February 14, 2020

Fixed alu files in the project and fixed alu symbols [1.5 hrs]

Monday, February 11, 2020

Added pass through functionality to the alu [2 hrs]

Wednesday, February 12, 2020

Worked on making better test cases for alu and started making sll module [3hrs]

My tasks for milestone 6 were to finish the test cases for the alu and the sll module, to assist in piecing the datapath together, and to compile the alu and the sll module.

**MILESTONE 5 WORK:**

Thursday, February 14, 2020

Finished sll module [3hrs](Verilog is hard)

Tuesday, February 18, 2020

Tested sll and added it to the alu. Then finished the alu test cases [3hrs]

Wednesday, February 19, 2020

Worked on computing the average cpi and helped with datapath [1.5hrs]

My tasks for the finished product is to help in attaching the architecture to a spartan board and testing to make sure everything works.